In the Claims:

Please amend the claims as indicated below.

1. (Currently Amended) Digital amplifier, comprising: a half bridge system with switches; a switching-timing correction circuit to which an input signal and an output signal of the switches is applied; wherein the switching-timing correction circuit is configured to indicate a first delay from timing differences between respective rising edges of the input and output signals, to indicate a second delay from timing differences between respective falling edges of the input and output signals, and to correct ~~corrects~~ switching timing errors of the switches responsive to an difference between the first delay and the second delay ~~on the basis of pulse-timing errors of the input signal of the switches and the output signal of the switches~~.

2. (Original) The digital amplifier of claim 1, wherein the switching-timing correction circuit corrects switching timing errors of the switches by delaying at least one of a rising edge and a falling edge of a pulse of the input signal.

3. (Currently Amended) The digital amplifier of claim 1, wherein the switching-timing correction circuit includes ~~comprises~~: a pulse edge delay detector for detecting the difference ~~an on/off-difference~~ between the first delay ~~an on-delay of a pulse supplied to the switches~~ and the second delay ~~an off-delay of the pulse response output by the switches~~; and an error signal generator for generating an error signal on the basis of the difference ~~on/off-difference~~; wherein the error signal corresponds to the pulse-timing errors between the input signal of the switches and the output signal of the switches; and wherein the switching-timing correction circuit corrects switching timing errors of the switches on the basis of the error signal.

4. (Original) The digital amplifier of claim 3, wherein the error signal is generated from one switching cycle and influences switching edges of a subsequent switching cycle.

5. (Original) The digital amplifier of claim 3, wherein the error signal is averaged

over a predetermined number of switching cycles by means of an averaging circuit to reduce a sub-harmonic injection.

6. (Original) The digital amplifier of claim 3, wherein the error signal is generated by means of an integration capacitor; and wherein the digital amplifier is a class D amplifier.

7. (Currently Amended) Switching-timing corrector for correcting switching timing errors of switches of a bridge of a digital amplifier, the switching-timing corrector comprising: a pulse edge delay detector for detecting a difference ~~an on/off-difference~~ between a first delay ~~an on-delay~~ of a pulse supplied to the switches and a second delay ~~an off-delay~~ of the pulse response output by the switches, the first delay representing a timing difference between a rising edge of the pulse and a rising edge of the pulse response, and the second delay representing a timing difference between a falling edge of the pulse and a falling edge of the pulse response; an error signal generator for generating an error signal on the basis of the difference ~~on/off-difference~~; an input pulse delay circuit for correcting switching timing errors of the switches by delaying at least one of a rising edge and a falling edge of a pulse of the input signal on the basis of the error signal.

8. (Original) The switching-timing corrector of claim 7, wherein the error signal is generated from one switching cycle and influences switching edges of a subsequent switching cycle.

9. (Original) The switching-timing corrector of claim 7, wherein the error signal is averaged over a predetermined number of switching cycles by means of an averaging circuit to reduce a sub-harmonic injection.

10. (Original) The switching-timing corrector of claim 7, wherein the error signal is generated by means of an integration capacitor; and wherein the switching-timing corrector is adapted for connection to a class D amplifier.

11. (Original) Method of correcting pulse-timing errors of switches of a bridge of a digital amplifier, the method comprising the steps of: detecting rising and falling pulse edges of an input and an output signal of the switches; generating an error signal corresponding to pulse edge delays between the rising and falling pulse edges of the input and the output signal; and correcting switching timing errors of the switches on the basis of the error signal.

12. (Original) The method of claim 11, wherein the switching timing errors of the switches are corrected by delaying at least one of the rising edge and the falling edge of a pulse of the input signal.

13. (Currently Amended) The method of claim 11, wherein the error signal is generated from one switching cycle and influences switching edges of a subsequent switching cycle, and further comprising indicating a first delay by measuring a timing difference between the rising edge of a pulse of the input signal supplied to the switches and the rising edge of a pulse of the output signal output by the switches responsive to the rising edge of the pulse of the input signal; and indicating a second delay by measuring a timing difference between the falling edge of the pulse of the input signal and the falling edge of the pulse of the output signal output by the switches responsive to the falling edge of the pulse of the input signal, wherein the error signal is generated responsive to determining the difference between the first delay and the second delay.

14. (Original) The method of claim 11, wherein the error signal is averaged over a predetermined number of switching cycles by means of an averaging circuit to reduce a sub-harmonic injection.

15. (Currently Amended) The switching-timing corrector of claim 7, wherein the pulse edge delay detector includes a first delay ~~an on-delay~~ measurement circuit that determines the first delay ~~on-delay from timing differences between rising edges of the input signal and the output signal~~, a second delay ~~an off-delay~~ measurement circuit that

determines the second delay ~~off-delay from timing differences between falling edges of the input signal and the output signal~~, and a subtractor that determines the difference between ~~on/off difference from~~ the first delay ~~on-delay~~ and the second delay ~~off-delay~~.

16. (Currently Amended) The switching-timing corrector of claim 15, wherein the error signal generator includes an integrator that integrates the difference ~~on/off-difference~~ to produce the error signal.

17. (Previously presented) The switching-timing corrector of claim 16, wherein the integrator is an integration capacitor.

18. (Previously presented) The switching-timing corrector of claim 7, wherein the switches of the bridge are MOSFETs, and wherein the input pulse delay circuit controls charging and discharging of each MOSFET gate capacities.

19. (Previously presented) The switching-timing corrector of claim 18, wherein for each MOSFET the input pulse delay circuit includes control circuitry that switches between current sources based on the input signal, one of the current sources being controlled by the error signal.

20. (New) The digital amplifier of claim 1, wherein the switching-timing correction circuit includes a first delay measurement circuit that indicates the first delay responsive to measuring a timing difference between a rising edge of a pulse of the input signal supplied to the switches and a rising edge of a pulse of the output signal output by the switches responsive to the rising edge of the pulse of the input signal, a second delay measurement circuit that indicates the second delay responsive to measuring a timing difference between a falling edge of the pulse of the input signal and a falling edge of the pulse of the output signal output by the switches responsive to the falling edge of the pulse of the input signal, and a subtractor that determines the difference between the first delay and the second delay.